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EXAMINER	
BRYANT, MICHAEL C	

ART UNIT	PAPER NUMBER
2884	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/532,119	PUHAKKA ET AL.	
	Examiner	Art Unit	
	CASEY BRYANT	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2009*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-29* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Applicant's reply, filed 10/14/2009, has been received and entered.

Claim 19, 23, 26 have been amended.

No claims have been cancelled.

No new claims have been added.

Thus, claims 1-29 remain currently pending in this application.

Response to Arguments

2. Applicant's arguments filed 10/14/2009 have been fully considered but they are not persuasive.

Regarding Priority Date of Spartiotis et al. (US 2003/0155516 A1)

The Spartiotis reference was non-provisionally filed in the US on May 23, 2002, predating the Applicant's priority date of October 23, 2002. It is noted that a rejection under 35 USC § 102(e) require that, "the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent." Therefore, the reference qualifies under 35 USC § 102(e). Due to the statute relied upon for the current grounds of rejection, a new grounds of rejection has been made.

Claim Rejections under 35 USC 102(a) over Spartiotis et al. (US 2003/0155516 A1)

Regarding claims 1, 2 and 11, the Applicant argues that Spartiotis fails to disclose cell circuitry located in a substrate that also includes the signal pathways. However, it is noted that the features upon which applicant relies (i.e., circuitry located in a substrate that also includes the signal pathways) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*,

988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Independent claims 1 and 11 merely recite that the semiconductor circuit substrate "comprises" each of the cell circuitry and signal pathways, and does not require the features to be collocated in the substrate.

The Applicant further argues that Spartiotis further fails to disclose conductive pathways coupled to the signal pathways. However, Spartiotis illustrates in Fig. 6A conductive pathways **136** coupled to the signal pathways **178** via conductive bonds **220** (0053, 0059). Furthermore as stated above, the claim does not require the elements to be collocated in the same substrate. However, because the claims are now rejected under 35 USC § 102(e), a new grounds of rejection has been made.

Claim Rejections under 35 USC 103(a) over Kyyhkynen (US 2002/0130266 A1) in view of secondary references

Regarding claims 1 and 11, in response to applicant's argument that Spartiotis fails to teach "a semiconductor circuit substrate comprising one or more signal pathways extending through the circuit substrate," the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Spartiotis discloses that forming an electrical connection through a circuit substrate is known in the art (Fig. 6A, 0051, 0057). Accordingly, it would have been obvious to one of ordinary skill in the art to use a via connection as taught by Spartiotis in the device of Kyyhkynen in place of the external electrical connection **83** (Fig. 4).

Regarding claims 19 and 26, as explained above regarding claims 1 and 11, the test for obviousness is not whether the features the claimed invention must be expressly suggested in any one or all of the references.

Spartiotis and Kyyhkynen are Properly Combinable References

Finally, Applicant argues that Spartiotis and Kyyhkynen are not properly combinable. Specifically, Applicant states that the combination would change the principle of operation of Kyyhkynen and would require a substantial reconstruction and redesign in order to incorporate the teachings of Spartiotis. But as recited above, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.

Kyyhkynen teaches an imaging system arranged use of the entire surface of the semiconductor detection substrate by providing an array of detector tiles super-positioned over wire bonds from each respective tile connecting readout to the circuitry below (Fig. 4). It is noted however, that the wire bond **83** requires enough substrate real estate such that the wire extends from a first connection on the readout substrate **42**, over the edge region of the substrate **42** to a second connection on the PCB mount **81**—that's two adjacent connections and the distance between the two connections for the wire. Spartiotis teaches that a via connection through a semiconductor substrate is known in the art, and are known to be used to increase the area of a detection substrate dedicated to imaging (0017, 0029, 0064). A via connection of the type disclosed by Spartiotis would require only a single connection space in the readout substrate **42** as opposed to the wire bond. Furthermore, the via connections taught by Spartiotis would not require substantially

altering the construction of the device, nor would it require a change in the basic principles under which the device of Kyyhkynen was designed to operate. Therefore the combination is proper.

Regarding the dependent claims and the second references relied upon, each of the rejections is maintained for at least the reasons presented above.

Claim Objections

3. Claim 29 is objected to because of the following informalities: the claim fails to end in a period. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Spartiotis et al. (US 2003/0155516 A1).

Regarding claims 1 and 11, Spartiotis discloses a system **80** comprising a detector substrate **90** having a plurality of detector cells **100** generating charge in response to incident radiation **hv**, each of the detector cells **100** including a cell contact **102** coupling charge from the detector cell to the semiconductor circuit substrate **170**; the semiconductor circuit substrate comprising a plurality of cell

circuit contacts **224**, each of which receives charge from a corresponding detector cell contact **102**, cell circuitry **132** associated with the plurality of cell circuit contacts **224**, conductive pathways **136** carrying readout signals to the cell circuitry **132**, and signal pathways **178** extending through the semiconductor circuit substrate **170**, the one or more signal pathways **178** being electrically coupled to the conductive pathways so as to provide an external signal interface for the cell circuitry **132** (Fig. 6A; 0051-53, 0060-61).

Regarding claim 2, Spartiotis discloses the signal pathways comprising via holes containing conductive material **184** (0057).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 5, 8-14, 16-19, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhkynen (US 2002/0130266 A1) in view of Spartiotis et al. (US 2003/0155516 A1).

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the

applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Regarding claims 1 and 11, Kyyhkynen discloses an x-ray detector tile (Fig. 4) comprising a detector substrate **44** having a plurality of detector cells **19** generating charge in response to incident radiation, each of the detector cells including a cell contact **54** coupling charge from the detector cell to a readout substrate **42** (0061-0062); the readout substrate comprising a plurality of cell circuit contacts, each of which receives charge from a corresponding detector cell contact, cell circuitry **20** associated with the plurality of cell circuit contacts, microbumps (i.e. conductive pathways) **46** arranged to carry a readout to cell circuitry, and a wire connection (signal pathway) **83** and the microbumps being electrically coupled so as to provide an external signal interface for the cell circuitry (Fig. 2 & 4; 0061-0062, 0074). Kyyhkynen does not disclose the signal pathway extending through the semiconductor circuit substrate. Spartiotis discloses an x-ray detector tile **80** comprising a signal pathway **178** formed through a substrate **170**, and providing a signal interface for detector cell circuitry **132** (Fig. 6A; 0051, 0057). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the signal pathway of Kyyhkynen as a via hole through the readout substrate, as taught by Spartiotis, in order to minimize dead area due to wire bonding in an x-ray detector tile (0017, 0029, 0064).

Regarding claim 2, Spartiotis discloses the signal pathway as a via hold containing conductive material (0057).

Regarding claim 5, Spartiotis discloses a conductive shielding around a substantial part of the signal pathway (via hole)(Fig. 10; 0056).

Regarding claims 8 and 9, Kyyhkynen discloses the readout substrate **42** comprising first and second opposing surfaces, the first surface proximate the detector substrate **44**, and wherein the cell circuit contacts are disposed on the first surface, and cell circuitry **20** is formed in a region of the first and second surface (Fig. 2&3; 0061-0062).

Regarding claim 10, Kyyhkynen discloses the cell circuitry comprising charge accumulation and readout circuitry (0064).

Regarding claim 12, Kyyhkynen discloses a bias contact **50** on a opposite surface of the detector cell contacts **54** (Fig. 2; 0062).

Regarding claim 13, Kyyhkynen discloses the bias contact as conductive (Fig. 2; 0062).

Regarding claims 14, Kyyhkynen discloses the detector substrate mechanically attached to the readout substrate by an array of microbumps **46** (Fig. 2; 0062).

Regarding claims 16, Kyyhkynen discloses a radiation detector tile **90** comprising a detection device **44/42** according to claim 11, and a mount **81** for mounting the detection device, wherein the mount includes contacts **83** for conductively connecting the conductive pathways to corresponding external signal lines disposed on the mount (0074).

Regarding claim 17, Kyyhkynen discloses a cassette **330** comprising a housing **350** and a plurality of radiation detection device tiles **90** according to claim 16, each tile being mounted in the housing and arranged so as to form an imaging tiled array (Fig. 9; 0097-0102).

Regarding claim 18, Kyyhkynen discloses at least a 3x3 array of detection tiles (Fig. 7).

Regarding claim 19, Kyyhkynen discloses a method of fabricating a semiconductor readout substrate **42**, the circuit substrate comprising cell circuitry, the method comprising: forming a signal pathway on the readout substrate having first and second ends, connecting a readout line **83** to the first end of the signal pathway, and connecting cell circuitry **20** to the second end of the signal pathway (Fig. 2&4; 0061-0064,0074). Kyyhkynen does not disclose forming the signal pathways as via holes through the substrate and depositing conductive material in the pathways to form conductive signal pathways. Spartiotis discloses a method of forming a signal pathway in a substrate comprising forming a via hole through the substrate depositing conductive material in the pathways to form conductive signal pathways (Fig. 6A; 0057). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the signal pathway of Kyyhkynen as a via hole through the readout substrate, as taught by Spartiotis, in order to minimize dead area due to wire bonding, especially in an x-ray detector tile (0017, 0029, 0064).

Regarding claim 24, Spartiotis discloses inserting conductive material into the via holes (0057).

Regarding claim 25, Kyyhkynen discloses a method of forming a detector device comprising: fabricating a readout substrate according to claim 19, forming a plurality or conductive contacts **46** on a surface of the readout substrate **42**, each contact arranged to receive charge from a detector cell **52** formed in a separate detector substrate **44**, connecting the plurality of conductive contacts with cell circuitry **20**, and connected the detector substrate to the readout substrate by means of the conductive contacts (Fig. 2; 0061-0064).

9. Claims 3, 4, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhkynen (US 2002/0130266 A1) in view of Spartiotis et al. (US 2003/0155516 A1) and Iwaki (US 2002/0180063 A1).

Regarding claim 3, Spartiotis discloses the readout substrate comprising a signal pathway but does not disclose the signal pathway extending through a region of lesser thickness than a first region. Iwaki discloses a semiconductor substrate comprising a via hole signal pathway formed in a region of lesser thickness that a surrounding region (Fig. 1; 0008). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the via hole signal pathway of Spartiotis in a substrate region of lesser thickness, as taught by Iwaki, in order to minimize the impedance of signal pathway.

Regarding claim 4, Iwaki discloses locating the region adjacent an edge of the substrate (Fig. 1).

Regarding claim 20, Spartiotis does not disclose reducing the thickness of the circuit substrate in a specific region and forming via holes through the region. Iwaki discloses forming a via hole signal pathway in a region of lesser thickness that a surrounding region of a substrate (Fig. 1; 0008). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the via hole signal pathway of Spartiotis in a substrate region of lesser thickness, as taught by Iwaki, in order to minimize the impedance of signal pathway.

Regarding claim 21, Spartiotis discloses forming circuitry in the circuit substrate prior to reducing the thickness (0006-0008).

10. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhkynen (US 2002/0130266 A1) in view of Spartiotis et al. (US 2003/0155516 A1) and Stratton et al. (US 6,952,042).

Regarding claim 6, Spartiotis discloses a via signal pathway comprising a conductive shielding, but does not disclose the conductive shield coupled to a reference potential. Stratton discloses a via hole held at a reference potential (col. 14, lines 4-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the conductive shield of Spartiotis at a reference potential in order to create a Faraday shield and collect parasitic noise/ions in the substrate.

Regarding claim 7, Stratton further discloses providing an insulating layer **514** between the conductive shield and adjacent conducting components (Fig. 5A; col. 7, lines 49-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an insulating layer between the via hole of Spartiotis and other conducting components in the device, as taught by Stratton, in order to isolate adjacent electrical elements (col. 6, lines 50-61).

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhkynen (US 2002/0130266 A1) in view of Spartiotis et al. (US 2003/0155516 A1) and Shahar et al. (US 2002/0036269 A1).

Regarding claim 15, Spartiotis discloses forming an adhesive layer between the detector and circuit substrates, the adhesive layer arranged to couple the detector and circuit substrates and preserve electrical contact between the detector cell contacts and signal pathways. Spartiotis does not disclose selectively exposing substantially all of each of the detector cell contacts of the detector substrate so as

to permit electrical contact between the signal pathways. Shahar discloses a patterning an adhesive **622** between a detector substrate **602** and circuit substrate **610** such that detector contacts **606** remain uncovered by the adhesive layer (Fig. 7; 0098). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the adhesive material between anode contacts of a detector in the confined inter-contact regions, as disclosed by Shahar, in the device of Spartiotis, in order to preserve continuous electrical contact between electrodes of the detector and circuit substrates, while reinforcing the adhesive coupling of the substrates.

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhkynen (US 2002/0130266 A1) in view of Spartiotis et al. (US 2003/0155516 A1) and Cho (US 5,937,326).

Regarding claim 23, Spartiotis discloses forming a plurality of via holes in a semiconductor substrate, but does not specify photolithographic methods. Cho discloses a method of forming a via hole in a semiconductor substrate comprising depositing photo-resist over the semiconductor substrate, applying a mask having an opening, exposing the photo-resist through the mask openings, removing the exposed photo-resist to expose the substrate, and etching the exposed semiconductor substrate so as to form the via hole (col. 1, line 57 – col. 2, line 30). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the method disclosed by Cho of forming a via hole in the device of Spartiotis, since photolithography is a well known cost-effective method of etching a precise patterns in a semiconductor device.

13. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spartiotis et al. (US 2003/0155516 A1) in view of Cho (US 5,937,326).

Regarding claim 26, Spartiotis discloses a method of fabricating a semiconductor imaging device **80**, the device comprising a semiconductor circuit substrate comprising cell circuitry, the method comprising: forming an array of via holes **178** through a circuit substrate **170** at locations associated with an array of detector cell circuit locations **132** (Fig. 6A), placing a detector substrate **90** having an array of detector cell contacts **102** corresponding to said array of cell circuit locations in relationship to the etched circuit substrate such that detector contacts are in correspondence with the via holes (Fig. 6A), and depositing a conductive material **184** in said via holes to provide signal pathways between said cell circuit locations and said detector cell contacts (Fig. 6A; 0051, 0056-0057). Spartiotis does not specifically disclose forming via holes in the circuit substrate using an etching step. Cho discloses a method of forming a via hole in a semiconductor substrate comprising etching a via hole using photolithographic methods (col. 1, line 57 – col. 2, line 30). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the method disclosed by Cho of forming a via hole in the substrate of Spartiotis, since photolithography is a well known cost-effective method of etching a precise pattern in a semiconductor device.

Regarding claim 27, Spartiotis discloses applying an adhesive material to the detector substrate and circuit substrate, and coupling the substrate by means of the adhesive material (0032).

14. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spartiotis et al. (US 2003/0155516 A1) in view of Cho (US 5,937,326) and Shahar et al. (US 2002/0036269 A1).

Regarding claim 28, Spartiotis discloses forming an adhesive layer between the detector and circuit substrates for adhesive coupling, but does not disclose patterning the adhesive to leave the contacts substantially uncovered by the adhesive. Shahar discloses a method of patterning an adhesive **622** between a detector substrate **602** and circuit substrate **610** such that detector contacts **606** remain uncovered by the adhesive (Fig. 7; 0098). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the adhesive material between anode contacts of a detector in the confined inter-contact regions, as disclosed by Shahar, in the device of Spartiotis, in order to preserve continuous electrical contact between electrodes of the detector and circuit substrates, while reinforcing the adhesive coupling of the substrates.

15. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spartiotis et al. (US 2003/0155516 A1) in view of Cho (US 5,937,326), Shahar et al. (US 2002/0036269 A1), and Nemirovsky et al. (US 6,645,787).

Regarding claim 29, Shahar discloses the adhesive material as comprising epoxy, but does not specify the material as comprising photoresist. Nemirovsky discloses a removable adhesive material **44** for coupling two a circuit substrate **40** with a detector substrate **11** as photoresist (Fig. 3; col. 6, lines 4-13). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the adhesive material of Shahar as photoresist, as taught by Nemirovsky, in order to

couple the circuit and detector substrate in a removable manner such that the contacts can be non-destructively detected for maintenance purposes.

Allowable Subject Matter

16. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 22, the prior art of record discloses forming via holes in a circuit substrate, and forming a conductive layer on the walls of the via hole (see Spartiotis). However, the prior of record fails to disclose or fairly suggest, in combination with the other claim steps, a method comprising depositing a conductive shielding over internal walls of via holes, and depositing an insulating layer over said conductive shielding.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CASEY BRYANT whose telephone number is (571)270-1282. The examiner can normally be reached on Monday - Friday, 8am - 5pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Porta/
Supervisory Patent Examiner, Art Unit 2884

Casey Bryant
Examiner